What is claimed is:

1. A method for making a semiconductor device comprising:

forming a conductive path on a substrate, the conductive path made of a first material;

depositing a second material on the conductive path; and

facilitating diffusion of the second material into the conductive path, the second material having a predetermined solubility to substantially diffuse to at least one of an interface and grain boundaries within the first material to significantly increase reliability of the conductive path.

2. The method of claim 1, wherein the first material comprises a metal.

3. The method of claim 2, wherein the metal is copper.

4. The method of claim 3, wherein forming the conductive path comprises a damascene process.

5. The method of claim 1, wherein depositing the second material comprises plating the second material on the conductive path.

6. The method of claim 5, wherein plating the second material comprises at least one of electroplating, electroless plating, and immersion plating the second material on the conductive path.

7. The method of claim 1 further comprising forming a barrier layer between the substrate and the conductive path.

8. The method of claim 1, wherein the substrate comprises an interlayer dielectric (ILD).

9. The method of claim 1, wherein the second material comprises a noble metal.

10. The method of claim 9, wherein the second material further comprises at least one of silver, gold, palladium, ruthenium, rhodium, osmium, iridium, and platinum.

11. The method of claim 1, wherein depositing the second material comprises depositing the second material subsequent to a planarization process of the substrate having the conductive path.

12. The method of claim 11, wherein depositing the second material comprises removing an oxide from the conductive path, and immersing the conductive path in an aqueous solution having at least the second material.

13. The method of claim 1, wherein depositing the second material comprises depositing the second material before a planarization process of the substrate having the conductive path.

14. The method of claim 13, wherein depositing the second material comprises removing an oxide from the conductive path, immersing the conductive path in an aqueous solution having at least the second material, and providing a planarization process of the substrate having the conductive path.

15. The method of claim 1, wherein facilitating diffusion of the second material comprises heat treating the conductive path having the deposited second material.

16. The method of claim 15, wherein heat treating the conductive path comprises annealing the conductive path at a predetermined temperature and time to substantially diffuse the second material to the grain boundaries within the first material, the predetermined temperature and time based at least in part on the first and second material.

17. The method of claim 1, wherein the conductive path comprises at least one of a conductive line and a conductive interconnect.

18. A semiconductor device comprising:

a conductive path formed on a substrate, the conductive path made of a first material; and

a second material deposited on the conductive path, the second material having a predetermined solubility to substantially diffuse to grain boundaries within the first material to significantly increase reliability of the conductive path.

19. The semiconductor device of claim 18, wherein the first material comprises a metal.

20. The semiconductor device of claim 19, wherein the metal is copper.

21. The semiconductor device of claim 20, wherein the conductive path comprises a conductive path formed by a damascene process.

22. The semiconductor device of claim 18 further comprising a barrier layer between the substrate and the conductive path.

23. The semiconductor device of claim 18, wherein the substrate comprises an interlayer dielectric layer (ILD).

24. The semiconductor device of claim 18, wherein the second material comprises a noble metal.

25. The semiconductor device of claim 24, wherein the second material further comprises at least one of silver, gold, palladium, ruthenium, rhodium, osmium, iridium, and platinum.

26. The semiconductor device of claim 18, wherein the conductive path comprises at least one of a conductive line and a conductive interconnect.